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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/808,059	03/24/2004	Leonard Forbes	400.285US01	4221

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EXAMINER	
PIZARRO CRESPO, MARCOS D	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 10/03/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/808,059	FORBES, LEONARD	
	Examiner	Art Unit	
	Marcos D. Pizarro-Crespo	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 July 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2 and 4-6* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2 and 4-6* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Attorney's Docket Number: 400.285US01
Filing Date: 3/24/2004
Claimed Foreign Priority Date: none
Applicant(s): Forbes
Examiner: Marcos D. Pizarro-Crespo

DETAILED ACTION

This Office action responds to the amendment filed on 7/6/2006.

Acknowledgment

1. The amendment filed on 7/6/2006, responding to the Office action mailed on 12/13/2005, has been entered. The present Office action is made with all the suggested amendments being fully considered. Accordingly, pending in this Office action are claims 1, 2 and 4-6.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claim 6 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

4. Claims 6 recites that the energy barrier at the interface between the high-k dielectric and the oxide is *larger than* the energy barrier at the interface between the oxide and the high-k dielectric. In other words, the energy barrier at said interface is larger than itself. The terms "*larger...than*" in claim 6 render the claim indefinite since

the energy barrier at the interface between the high-k dielectric and the oxide cannot be larger than the energy barrier at that very same interface. The specification provides no disclosure specifying an interface between the high-k dielectric and the oxide having two different energy barrier values. It is not clear what it is that the applicants are trying to compare and one of ordinary skill in the art would not be reasonably appraised of the scope of the invention with regards to claim 6.

Claims Rejection

5. Initially, and with respect to claims 1, 2, and 4-6, note that a "product by process" claim is directed to the product *per se*, no matter how actually made. See *In re Thorpe*, 227 USPQ 964 (CAFC, 1985) and the related case law cited therein which makes it clear that it is the final product *per se* which must be determined in a "product by process" claim, and not the patentability of the process, and that, as here, an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. As stated in Thorpe,

> even though product-by-process claims are limited by and defined by the process, determination of patentability is based on the product itself. *In re Brown*, 459 F.2d 531, 535, 173 USPQ 685, 688 (CCPA 1972); *In re Pilkington*, 411 F.2d 1345, 1348, 162 USPQ 145, 147 (CCPA 1969); *Buono v. Yankee Maid Dress Corp.*, 77 F.2d 274, 279, 26 USPQ 57, 61 (2d. Cir. 1935).

Note that the applicants have the burden of proof in such cases, as the above case law makes clear.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1, 2, and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sugizaki in view of Yu (US 6495437).

8. Regarding claim 1, Sugizaki shows (see, *e.g.*, fig. 1) most aspects of the instant invention including an NROM memory transistor comprising:

- ✓ A substrate
- ✓ A plurality of source/drain regions with a different conductivity than the substrate
- ✓ A nanolaminate, high-permittivity (high-k), metal-oxide gate-dielectric composed of oxide–aluminum oxide–oxide and overlying the substrate
- ✓ A control gate formed on top of the gate dielectric

9. Regarding claim 2, Sugizaki shows (see, *e.g.*, fig. 1) the gate dielectric is a composite oxide–high k dielectric–oxide nanolaminate gate insulator wherein the high-k dielectric is a charge trapping layer.

10. Regarding claim 5, Sugizaki teaches that the charge-trapping layer comprises a material, Al_2O_3, which has a lower conduction band edge than silicon nitride (see, *e.g.*, pp.27/ll.41-51).

11. Regarding claims 1 and 2, it is noted that Sugizaki shows all aspects of the semiconductor device according to the claimed invention (see, *e.g.*, paragraphs 9-11 above) and that the method of forming aluminum oxide by the low-temperature oxidation of aluminum, is an intermediate step that does not affect the structure of the final device.

In spite of the above, Yu (see, *e.g.*, col.7/ll.23-33) teaches using a low-temperature oxidation step to form the aluminum oxide of Sugizaki as an oxidized aluminum gate dielectric. Yu teaches that doing so would result in a substantial uniform thickness for the gate dielectric and that although other processes may be used such are not preferred as they may result in undesirable non-uniform thicknesses for the gate dielectric (see, *e.g.*, col.7/ll.33-38).

Accordingly, it would have been obvious at the time of the invention to one of ordinary skill in the art to form Sugizaki's aluminum oxide by the low temperature oxidation of a metal, as suggested by Yu, because doing so would result in a gate dielectric having a substantial uniform thickness.

12. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sugizaki/Yu in view of Akatsu (US 5717635).

13. Regarding claim 4, Sugizaki/Yu shows most aspects of the instant invention (see, *e.g.*, paragraph 8 above). They, however, fail to show that the transistor is in either a NOR-type flash memory structure of a NAND-type flash memory structure. Sugizaki, however, teaches that the transistor is a flash memory device (see, *e.g.*, abstract). At the present time, there are two basic architectures for memory cell arrays referred to as

NOR-type and NAND-type respectively (see, *e.g.*, Akatsu/col.4/ll.50-57). The NAND-type, however, lends itself to much higher integration densities (see, *e.g.*, Akatsu/col.5/ll.34-40).

It would have been obvious at the time of the invention to one of ordinary skill in the art to have Sugizaki/Yu's transistor in a NAND-type memory structure, as suggested by Akatsu, to achieve high-integration density.

Response to Arguments

14. The applicant argues:

Sugizaki teaches a memory using a high-k charge-trapping layer. He, however, fails to show applicant's final structure that results from the low temperature oxidation of aluminum. Sugizaki differently teaches chemical vapor deposition (CVD) to form the trapping layer. It is well known that the oxidized aluminum results in a more uniform structure than is achievable by CVD. In addition, the structure formed by the low temperature oxidation results in a higher tunnel barrier on the interface between the oxidized metal layer and the top insulator than between the oxidized metal layer and the tunnel insulator (see, e.g., par.0046). Further, par.0053 of the present specification discusses the electrical differences between the low temperature oxidation structure and Sugizaki's CVD structure.

The examiner responds:

Applicant's arguments are mainly directed to process aspects of the claimed invention. The claims, however, are directed to a structure not to a process. The process terminology is considered only in terms of a necessary resultant from the process. The process itself is not at issue. The recited process does not limit the device claims. See MPEP § 2113; *In re Brown*, 173 USPQ 685 (CCPA 1972); *In re Fitzgerald*, 205 USPQ 594 (CCPA 1980); *In re Marosi*, 218 USPQ 289, 292-293 (CCPA 1983); *In re Thorpe*, 227 USPQ 964 (CAFC 1985).

In spite of the above, Yu (see, *e.g.*, col.7/ll.23-33) teaches using a low-temperature oxidation step to form the aluminum oxide of Sugizaki as an oxidized aluminum gate dielectric. Yu teaches that doing so would result in a substantial uniform thickness for the gate dielectric and that although other processes may be used such are not preferred as they may result in undesirable non-uniform thicknesses for the gate dielectric (see, *e.g.*, col.7/ll.33-38).

Accordingly, it would have been obvious at the time of the invention to one of ordinary skill in the art to form Sugizaki's aluminum oxide by the low temperature oxidation of a metal, as suggested by Yu, because said oxidation is recognized in the art as a preferred process step that would result in the gate dielectric having a substantial uniform thickness.

Conclusion

15. Papers related to this application may be submitted directly to Art Unit 2814 by facsimile transmission. Papers should be faxed to Art Unit 2814 via the Art Unit 2814 Fax Center. The faxing of such papers must conform to the notice published in the Official Gazette, 1096 OG 30 (15 November 1989). The Art Unit 2814 Fax Center number is **(571) 273-8300**. The Art Unit 2814 Fax Center is to be used only for papers related to Art Unit 2814 applications.

16. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Marcos D. Pizarro-Crespo** at **(571) 272-1716** and between the hours of 10:00 AM to 8:30 PM (Eastern Standard Time) Monday through Thursday or by e-mail via Marcos.Pizarro@uspto.gov. If attempts to reach the

examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy, can be reached on (571) 272-1705.

17. Any inquiry of a general nature or relating to the status of this application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

18. The following list is the Examiner's field of search for the present Office Action:

Field of Search	Date
U.S. Class / Subclass(es): 257/314,324-326,410,411	9/28/2006
Other Documentation:	
Electronic Database(s): EAST (USPAT, EPO, JPO)	9/28/2006

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